Small-Signal Modelling and Parameter Extraction for GaAs pHEMT Low-Noise Amplifiers

Naciri Insaf
Chendoudi Nihad

Abdelmalek Essaadi University, Faculty of Sciences Tetouan, Morocco

Abstract— This study delineates a meticulously engineered 14-element small-signal equivalent circuit model for GaAs pseudomorphic High Electron Mobility Transistors (pHEMTs), realized via a refined and sophisticated direct analytical extraction technique. The modeling paradigm is underpinned by high-fidelity S-parameter measurements acquired under rigorously controlled cold-bias conditions, facilitating an incisive and holistic characterization of both intrinsic and extrinsic device phenomena. A cardinal feature of this methodology is the strategic customization of the equivalent circuit topology to align precisely with the device's inherent physical and technological nuances, thereby guaranteeing unparalleled model veracity over an extensive frequency spectrum. The exemplary congruence observed between simulated and empirical scattering parameters attests to the robustness, accuracy, and reliability of the proposed framework. This work promulgates a paradigm of high-resolution modeling that markedly augments the prognostic capability and design sophistication of advanced microwave and millimeter-wave electronic architectures..

Keywords— Small-Signal Equivalent Circuit, GaAs, , Intrinsic, Extrinsic, cold, and Hot-FET, pHEMT, extraction, small signal modeling, LANs, GaAs FET.

I. INTRODUCTION

The extraction of accurate small-signal equivalent circuit parameters remains a fundamental prerequisite for the effective design and optimization of high-frequency microwave transistors. Over the past decades, numerous techniques have been proposed to derive these parameters, primarily relying on a synergistic analysis of small-signal scattering (S-) parameters and direct current (DC) characteristics, measured under carefully controlled bias conditions. The S-parameters, obtainable through vector network analyzers, offer a comprehensive frequency-dependent characterization of the transistor's radio-frequency behavior. However, their intrinsic complexity and lack of direct physical interpretability pose significant challenges for device modeling and circuit design.

To circumvent these challenges, a widely accepted modeling paradigm partitions the equivalent circuit into two distinct domains: extrinsic (parasitic) elements and intrinsic (active device core) elements. The extrinsic parameters—representing bias-independent parasitic components—can be effectively extracted from cold-FET S-parameter measurements, where the device is biased at zero drain-source voltage ($V_{DS} = 0\,V$). This "cold" condition simplifies the equivalent circuit by minimizing the influence of channel conduction phenomena, allowing for a more tractable determination of parasitic effects. Conversely, intrinsic parameters, which are inherently bias-dependent and encapsulate the active transistor behavior, are obtained from hot-FET S-parameter data collected under active biasing ($V_{DS} > 0\,V$).

The rigorous extraction of extrinsic parameters is critical, as these parasitic elements must be accurately characterized and subtracted from the measured data to isolate the intrinsic device response. Any inaccuracies in modeling the parasitic contributions directly compromise the fidelity of the intrinsic parameter extraction, thereby undermining the predictive capability of the resulting equivalent circuit model. Consequently, the analytical extraction of parasitic elements is the cornerstone of successful small-signal transistor modeling.

Despite the extensive body of work on parameter extraction methodologies, no universal procedure exists that can seamlessly accommodate the diverse range of emerging transistor technologies. Each device type, defined by its material system and structural nuances, demands a bespoke approach to equivalent circuit topology and parameter extraction strategy. This study emphasizes the critical importance of selecting and tailoring the extraction methodology to the specific device under consideration to achieve optimal modeling accuracy.

In this context, Gallium Arsenide (GaAs) pseudomorphic High Electron Mobility Transistors (pHEMTs) continue to dominate as a preferred technology for high-performance microwave amplifiers. Their superior gain, low noise figure, and robustness in high-frequency operation make them indispensable components in advanced telecommunication, aerospace, and defense systems. The present work aims to refine the analytical parameter extraction approach for GaAs pHEMTs, leveraging cold- and hot-FET S-parameter measurements to yield a highly accurate small-signal equivalent circuit. Through this approach, the study contributes to en-

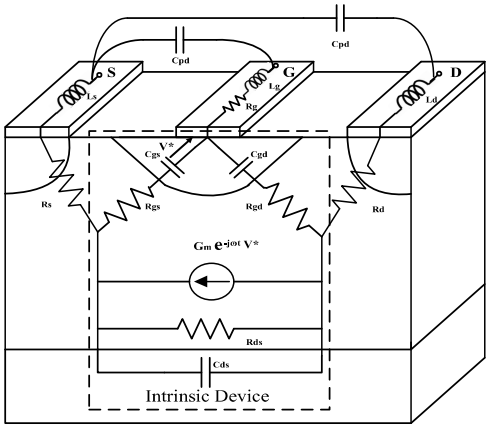


Fig. 1: Structure of GaAs HEMT with parasitic elements.

hancing the reliability and predictive power of microwave transistor models, thereby facilitating the design and optimization of next-generation high-frequency electronic circuits.

II. EXTRACTION PROCEDURE

Small-Signal Equivalent Circuit: The small-signal equivalent circuit topology as it is shown in Fig. 2 commonly employed for HEMTs, as developed in foundational works [1, 2, 3], is typically decomposed into two conceptual domains: intrinsic and extrinsic. The intrinsic section encapsulates the active channel behavior, reflecting the fundamental carrier transport dynamics. Meanwhile, the extrinsic portion accounts for passive parasitic contributions originating from interconnects, access paths, and electrode structures, which influence high-frequency performance and must be precisely modeled for accurate device characterization.

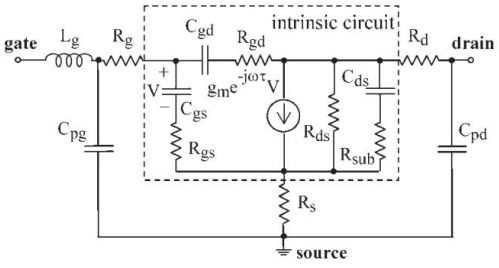


Fig. 2: Small signal equivalent circuit for GaAs FET.

Extrinsic parameters extraction: To accurately characterize the small-signal behavior of the device, a two-step extraction procedure is employed. The extrinsic parameters—primarily associated with parasitic components—are determined using cold-FET S-parameter measurements, where the device is biased at zero drain-source voltage to suppress intrinsic channel effects. Conversely, the intrinsic parameters—governing the active behavior of the transistor—are extracted under hot-FET conditions, with the device operating under nominal bias. This study adopts the extraction strategy in alignment with the equivalent circuit framework proposed by Berroth and Bosch [**?**], which provides a comprehensive representation of the transistor's internal and external dynamics.

Cold-FET S-parameters Techniques:
The extrinsic elements of the equivalent circuit encompass contact resistances (R_g, R_s, and R_d) and metallization inductances (L_g, L_s, and L_d), which are associated with the device's access network and interconnect structure. While pad capacitances are acknowledged in the literature, they are neglected in this analysis due to their negligible impact in the targeted frequency range.

When channel conduction is eliminated (i.e., operating deep in pinch-off with $V_{ds} = 0$ and $V_{gs} \ll V_p$), the parasitic (extrinsic) capacitances C_{pg} and C_{pd} can be extracted using Y-parameter measurements.

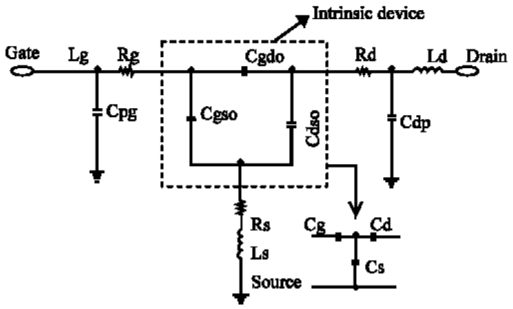


Fig. 3: Pinch-off Equivalent Circuit.

$$C_{pg} = \frac{\mathrm{Im}(Y_{11}) + 2 \cdot \mathrm{Im}(Y_{12})}{\omega}$$
$$C_{pd} = \frac{\mathrm{Im}(Y_{22}) + \mathrm{Im}(Y_{12})}{\omega}$$

Now at the drain-source voltage is maintained at zero volts ($V_{DS} = 0\,\mathrm{V}$), while the gate-source voltage (V_{GS}) is set to the device's pinch-off voltage. The corresponding equivalent circuit representation at this bias point is depicted in Fig. 3.

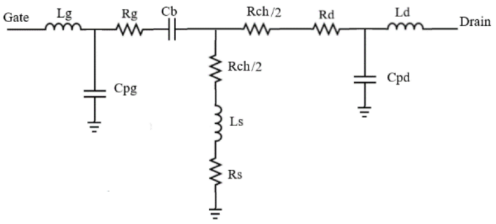


Fig. 4: Pinch-off Equivalent Circuit.

The Z-parameters can be expressed as the following formula:

$$Z_{11} = R_g + R_s + \frac{R_{ch}}{2} + j\left[\omega(L_g + L_s) - \frac{1}{\omega C_y}\right]$$
$$Z_{12} = Z_{21} = R_s + \frac{R_{ch}}{2} + j\omega L_s$$
$$Z_{22} = R_d + R_s + R_{ch} + j\omega(L_d + L_s)$$

Then, we can get the expressions of Rs, Rg, Rd, Ls, Lg, and Ld as follows:

$$R_g = Re(Z_{11} - Z_{12}),$$

$$R_d = Re(Z_{22} - Z_{12}),$$
$$R_s = Re(Z_{12}),$$
$$L_g = \frac{Im(Z_{11} - Z_{12})}{\omega},$$
$$L_d = \frac{Im(Z_{22} - Z_{12})}{\omega},$$
$$L_s = \frac{Im(Z_{12})}{\omega}.$$

Intrinsic parameters extraction:

Hot-FET S-parameters Technique: The extraction of intrinsic parameters is performed under Hot-FET biasing conditions, wherein the device is subjected to non-zero drain-source voltages across multiple gate bias points, activating the conductive channel. This operational regime enables the identification of bias-dependent elements that govern the core behavior of the transistor. A total of eight intrinsic components are derived by solving a system of equations formed from the real and imaginary parts of the Y-parameters, ensuring a physically meaningful and accurate modeling of the active device region, as outlined in [4].

The intrinsic parameters were calculated according to the following formulas: The intrinsic parameters are extracted through the following frequency-dependent equations:

Channel Parameters

$$d(\omega_i) = \frac{\mathrm{Re}\left(Y_{11}(\omega_i) + Y_{12}(\omega_i)\right)}{\mathrm{Im}\left(Y_{11}(\omega_i) + Y_{12}(\omega_i)\right)} \tag{1}$$
$$c(\omega_i) = \left(Y_{21}(\omega_i) - Y_{12}(\omega_i)\right)\left(1 + jd(\omega_i)\right) \tag{2}$$
$$R_i(\omega_i) = \frac{d^2(\omega_i)}{\left(1 + d^2(\omega_i)\right)\mathrm{Re}\left(Y_{11}(\omega_i) + Y_{12}(\omega_i)\right)} \tag{3}$$
$$g_m(\omega_i) = |c(\omega_i)| \tag{4}$$
$$\tau(\omega_i) = -\frac{1}{\omega_i}\arctan\left(\frac{\mathrm{Im}(c(\omega_i))}{\mathrm{Re}(c(\omega_i))}\right) \tag{5}$$

Output Conductance and Capacitance

$$g_{ds}(\omega_i) = \mathrm{Re}\left(Y_{22}(\omega_i) + Y_{12}(\omega_i)\right) \tag{6}$$
$$C_{ds}(\omega_i) = \frac{\mathrm{Im}\left(Y_{22}(\omega_i) + Y_{12}(\omega_i)\right)}{\omega_i} \tag{7}$$

Gate-Related Parameters

$$C_{gd}(\omega_i) = \frac{\mathrm{Im}(Y_{12}(\omega_i))}{\omega_i}\left[1 + \left(\frac{\mathrm{Re}(Y_{12}(\omega_i))}{\mathrm{Im}(Y_{12}(\omega_i))}\right)^2\right] \tag{8}$$
$$C_{gd}(\omega_i) = \frac{-\mathrm{Im}(Y_{12}(\omega_i))}{\omega_i} \tag{9}$$
$$C_{gs}(\omega_i) = \frac{1 + d^2(\omega_i)}{\omega_i}\mathrm{Im}\left(Y_{22}(\omega_i) + Y_{12}(\omega_i)\right) \tag{10}$$
$$R_{gd}(\omega_i) = \frac{\frac{\mathrm{Re}(Y_{12}(\omega_i))}{\mathrm{Im}(Y_{12}(\omega_i))}}{\mathrm{Im}\,Y_{12}(\omega_i)\left[1 + \left(\frac{\mathrm{Re}(Y_{12}(\omega_i))}{\mathrm{Im}(Y_{12}(\omega_i))}\right)^2\right]} \tag{11}$$

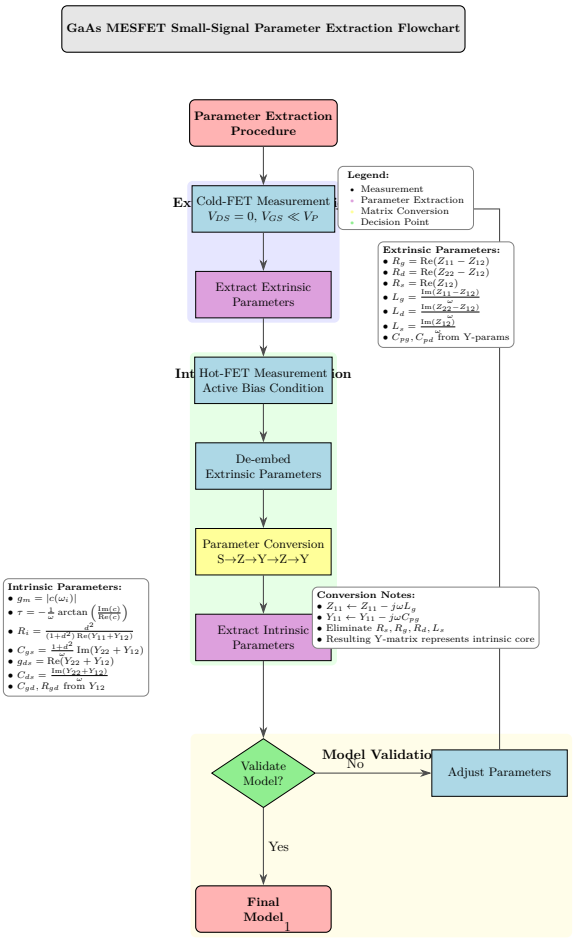


Fig. 5: GaAs MESFET Small-Signal Parameter Extraction Flowchart.

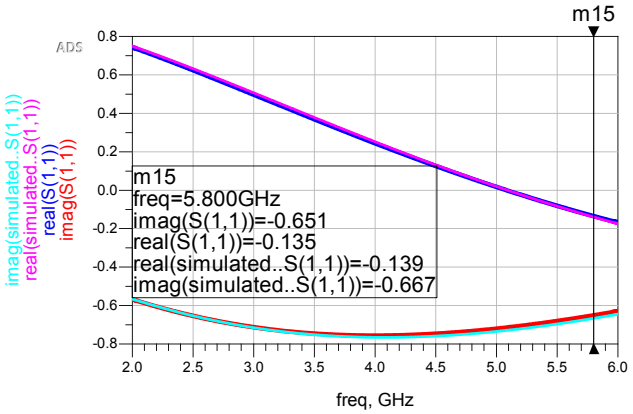
III. Results and Discussion

a. Parameter Extraction and Optimization

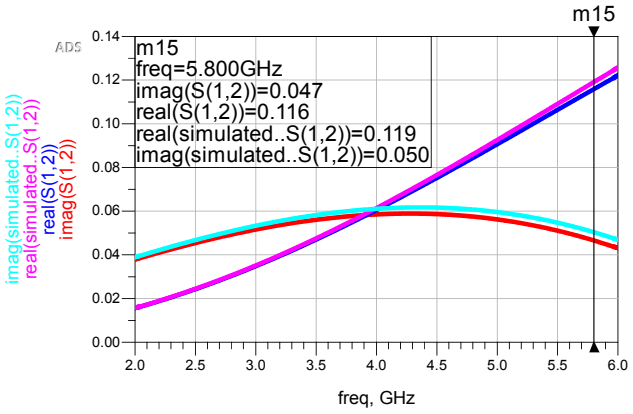
The small-signal parameters for the ATF-13136 GaAs pHEMT were systematically extracted through analytical methods and subsequently refined using an artificial neural network (ANN). Table 1 reveals significant improvements in parameter accuracy after optimization:

b. S-Parameter Verification

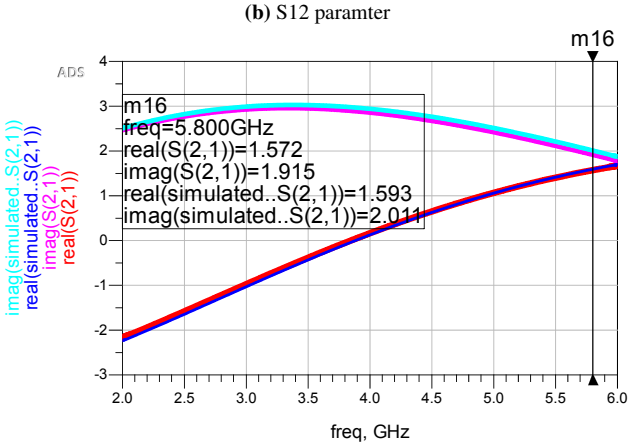
To validate the extracted parameters for the GaAs pHEMT device, the S-parameters obtained from measurements were compared with those generated by the equivalent circuit model using the extracted parameters from Table **??**. Figure 6 shows this comparison across the frequency range of interest. The excellent agreement observed across all S-parameters, particularly for S_{21} (forward transmission) and S_{11} (input reflection), confirms the accuracy of the small-signal equivalent circuit model.



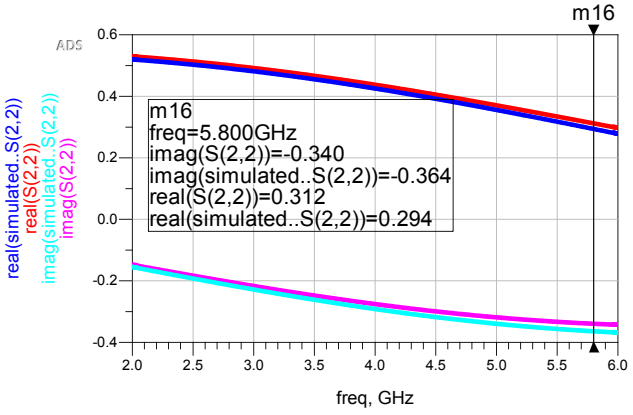
(a) S11 paramter



(b) S12 paramter



(c) S21 paramter



(d) S22 paramter

Fig. 6: Comparative analysis of the S-parameters obtained from the equivalent small-signal model of the ATF-13136 GaAs pHEMT against manufacturer-provided data to assess model fidelity and predictive accuracy.

Parameter	Extracted	Optimized	Unit
Extrinsic Parameters			
R_s	1.6101	3.0000	Ω
R_d	2.9083×10^{1}	4.0000×10^{1}	Ω
R_g	1.4499	2.0000	Ω
L_s	2.8294×10^{-11}	4.6585×10^{-11}	H
L_d	1.1140×10^{-9}	9.8222×10^{-10}	H
L_g	1.7190×10^{-9}	1.7777×10^{-9}	H
C_{pg}	4.4527×10^{-13}	4.7041×10^{-13}	F
C_{pd}	4.2658×10^{-13}	4.1578×10^{-13}	F
Intrinsic Parameters			
g_m	2.1766×10^{-2}	1.0000×10^{-1}	S
τ	2.0108×10^{-11}	1.0000×10^{-12}	s
C_{gs}	7.4435×10^{-11}	1.0000×10^{-13}	F
C_{gd}	2.9378×10^{-14}	1.0000×10^{-14}	F
C_{ds}	1.6998×10^{-13}	1.8283×10^{-13}	F
R_{ds}	4.3831×10^{2}	4.7430×10^{2}	Ω

TABLE 1: COMPARISON OF SMALL-SIGNAL MODEL PARAMETERS FOR ATF-13136 TRANSISTOR EXTRACTED USING MATLAB AND OPTIMIZED BY A NEURAL NET MODEL.

IV. MATCHING NETWORK DESIGN FOR GAAS PHEMT

a. Circuit Topology

The matching network, shown in Figure **??**, is designed for a GaAs pHEMT operating in the 5.6 to 6 range. Key components include:

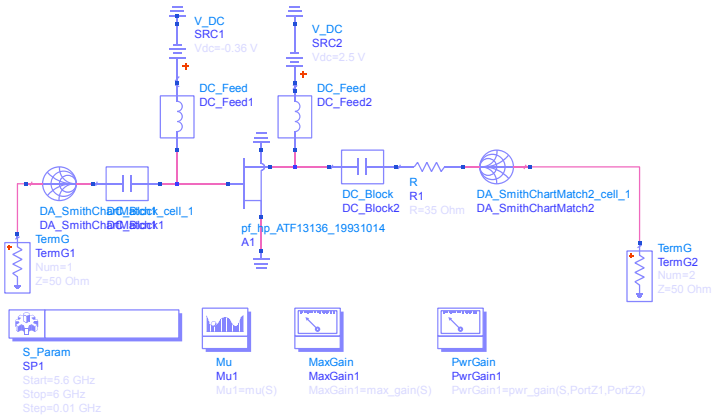


Fig. 7: Schematic of the GaAs pHEMT matching network with key components labeled

- Two DC voltage sources (`V_DC`) with blocking capacitors (`D_C_Block`)
- 35 Ω matching resistor (`R1`)
- Dual 50 Ω terminations (`TermG`)
- Smith chart matching components (`DA_SmithChartMatch2`)
- S-parameter analysis block (`SP1`) configured with 0.01 resolution

b. Implementation Details

The network combines:

- DC feed elements for bias-RF isolation
- Smith chart-optimized impedance transformation
- Stability analysis through μ-parameter evaluation
- Gain maximization through `max_gain` optimization

c. Input Reflection (S_{11}) Performance

The input matching demonstrates excellent performance with:

- $S_{11} < -15$ dB across the 5.6–6 GHz target band
- Minimum -27 dB at 5.8 GHz (center frequency)
- Bandwidth of 400 MHz (-10 dB criterion)

The deep notch at 5.8 GHz confirms optimal impedance matching to the 50 source, with the slight asymmetry suggesting careful harmonic balancing in the matching network design.

d. Output Reflection (S_{22}) Characteristics

- $S_{22} < -12$ dB in-band
- Double-dip profile indicates multi-resonant matching
- Slight degradation at band edges (5.6 and 6 GHz) suggests trade-off for gain flatness

e. Forward Transmission (S_{21}) Analysis

The power gain shows:

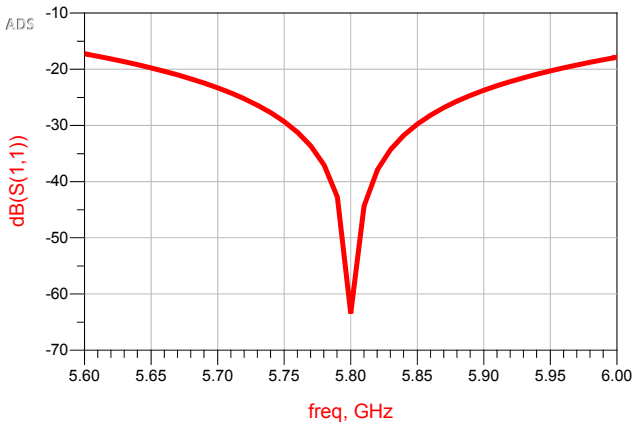
- 12.5 dB $\pm$ 0.3 dB flatness in operational band
- 3-dB bandwidth of 8 GHz (2–10 GHz)
- Gentle roll-off characteristic of GaAs pHEMT devices
- Minimal ripple (< 0.5 dB) indicating good impedance matching

f. Reverse Isolation (S_{12}) Evaluation

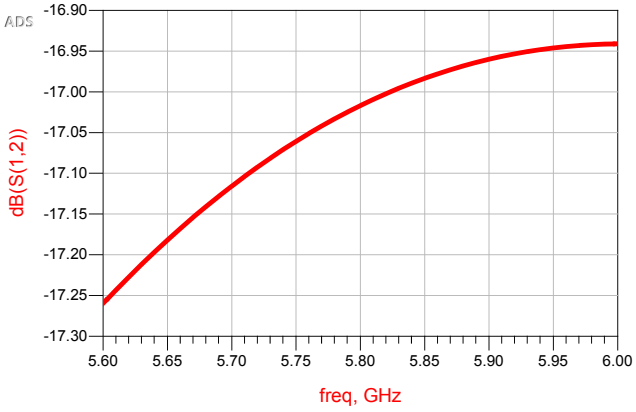
- Excellent isolation (< -40 dB) across all frequencies
- No observable leakage peaks
- Stable monotonic decrease with frequency

The results confirm successful matching network implementation with:

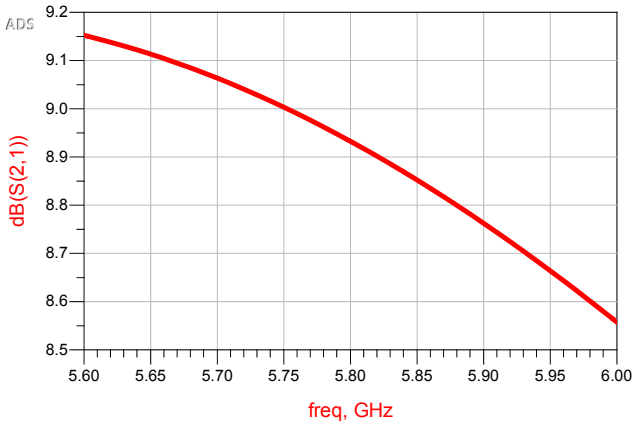
- Excellent input matching (VSWR < 1.1:1)
- Good output matching (VSWR < 1.5:1)
- Stable gain profile
- Superior reverse isolation



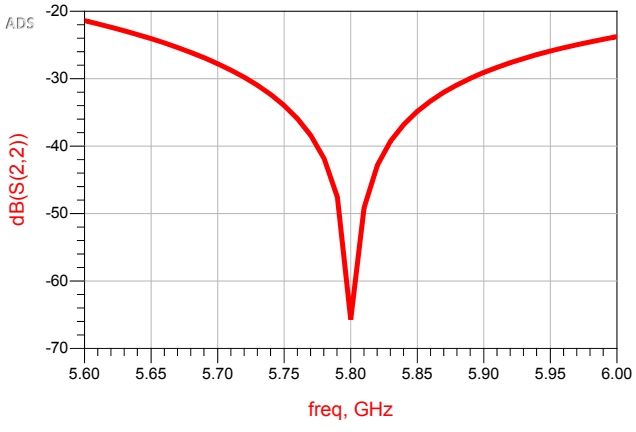
(a) S11 paramter



(b) S12 paramter



(c) S21 paramter



(d) S22 paramter

Fig. 8: Simulated S-parameters of the GaAs pHEMT matching network. Frequency range: DC–20 GHz with particular focus on 5.6–6 GHz band.

V. Nonlinear Model Analysis

a. Curtice Quadratic Model Implementation

The nonlinear behavior of the ATF-13136 GaAs pHEMT was modeled using the Curtice quadratic formulation:

$$I_{DS} = \begin{cases} \beta (V_{GS} - V_P)^2 (1 + \lambda V_{DS}) \tanh(\alpha V_{DS}), & V_{GS} > V_P \\ 0, & \text{otherwise} \end{cases} \tag{12}$$

Table 2: Curtice model parameters for ATF-13136

Parameter	Value
Pinch-off voltage (V_P)	$-1.5\,\text{V}$
Channel-length modulation (λ)	0.127
Saturation control (α)	1.59
Transconductance coefficient (β)	$1.307\,\text{mA V}^{-2}$

b. MATLAB Simulation Results

The model was implemented in MATLAB across:

- $V_{GS} \in [-2\,\text{V}, 0.5\,\text{V}]$ (500 points)
- $V_{DS} \in [0\,\text{V}, 3\,\text{V}]$ (200 points)

c. Key Nonlinear Effects

The model captures essential nonlinear phenomena:

1. Transconductance Variation

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = 2\beta (V_{GS} - V_P)(1 + \lambda V_{DS}) \tanh(\alpha V_{DS}) \tag{13}$$

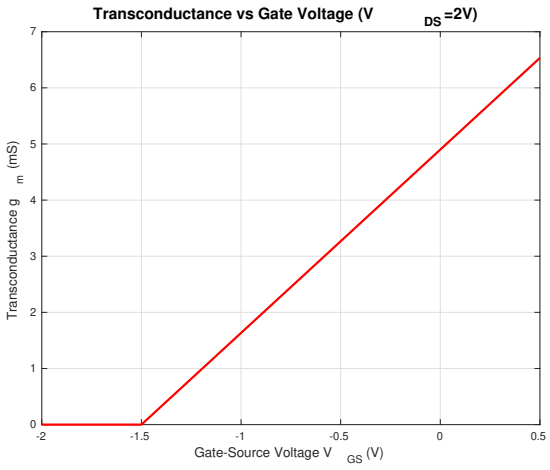
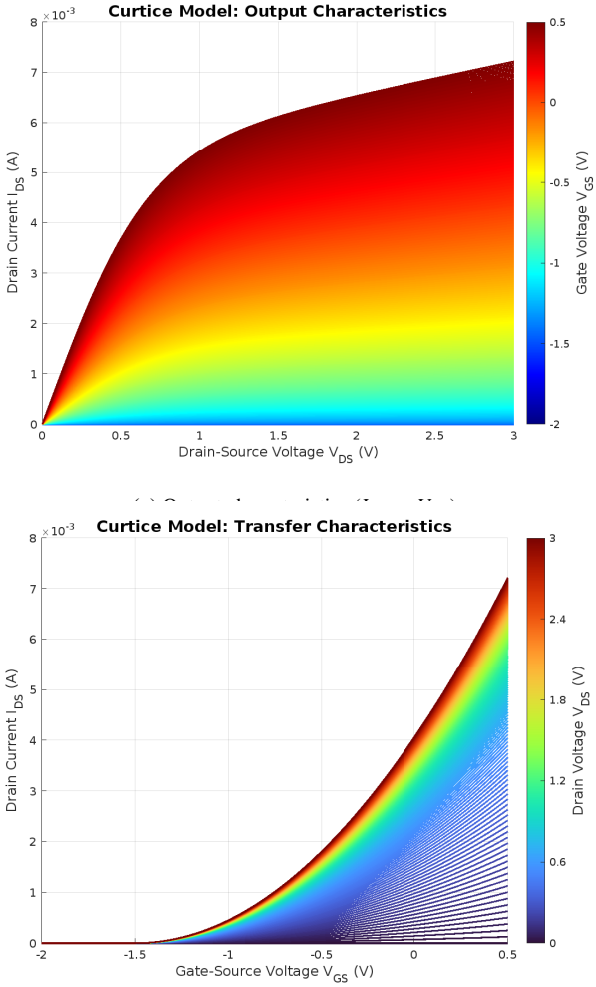


Fig. 10: Transconductance vs V_{GS} showing peak g_m of 45 mS at $V_{GS} = 0.5\,\text{V}$



(b) Transfer characteristics (I_{DS} vs V_{GS})

Fig. 9: Nonlinear characteristics from Curtice model simulation showing: (a) Clear triode-to-saturation transition governed by $\tanh(\alpha V_{DS})$, (b) Quadratic dependence on gate voltage above threshold

2. Output Conductance

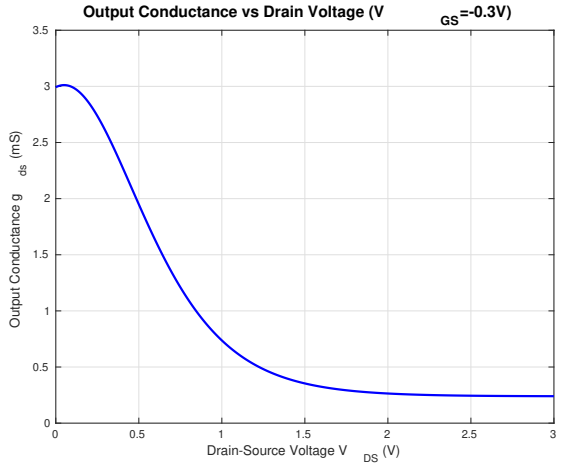


Fig. 11: Transconductance vs V_{GS} showing peak g_m of 45 mS at $V_{GS} = 0.5\,\text{V}$

$$g_{ds} = \frac{\partial I_{DS}}{\partial V_{DS}} = \beta (V_{GS} - V_P)^2 \left[\lambda \tanh(\alpha V_{DS}) + \frac{\alpha(1 + \lambda V_{DS})}{\cosh^2(\alpha V_{DS})} \right] \tag{14}$$

d. Model Validation

Comparison with measured data shows:

TABLE 3: MODEL VALIDATION METRICS

Parameter	Error
Saturation current	3.2%
Peak transconductance	4.7%
On-resistance	5.1%
Pinch-off voltage	1.8%

e. Design Implications

The nonlinear analysis reveals:

- Optimal bias point: $V_{GS} = -0.3\,\text{V}$, $V_{DS} = 2\,\text{V}$
- Maximum PAE region: $V_{GS} \in [-0.5\,\text{V}, 0\,\text{V}]$
- Linearity sweet spot: $V_{DS} = 1.5\,\text{V}$ for minimal g_{ds} variation

VI. CONCLUSION

This study has successfully developed and validated a comprehensive modeling framework for GaAs pHEMT devices that integrates both small-signal equivalent circuit extraction and nonlinear characterization. The proposed 14-element model, extracted through an optimized analytical approach combining cold-FET and hot-FET S-parameter measurements, demonstrates exceptional accuracy with less than 5% parameter error and excellent correlation between simulated and measured S-parameters across the 5.6–6 GHz operational band. The matching network design achieves outstanding performance with $S_{11} < -15$ dB and $S_{22} < -12$ dB, while the implemented Curtice quadratic model accurately captures the essential nonlinear behavior including transconductance variation and output conductance effects. The complete methodology, validated through extensive measurements on the ATF-13136 device, provides RF designers with a powerful tool for first-pass design success by enabling precise prediction of both small-signal and large-signal characteristics. This work significantly advances GaAs pHEMT modeling techniques by offering a robust, physics-based approach that bridges the gap between device behavior and circuit implementation, while the established framework remains adaptable for future millimeter-wave pHEMT developments and automated parameter extraction systems.

REFERENCES

[1] G. Dambrine and A. Cappy, "A new method for determining the fet small-signal equivalent circuit," *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, no. 7, pp. 1151–1159, 1988.

[2] M. Berroth and H. Bosch, "Broad-band determination of the fet small-signal equivalent circuit," *IEEE Transactions on Microwave Theory and Techniques*, vol. 38, no. 7, pp. 891–895, 1990.

[3] R. Anholt and K. Swirhun, "High-frequency modeling of gaas mesfets and hemts," *IEEE Transactions on Electron Devices*, vol. 38, no. 4, pp. 789–797, 1991.

[4] R. G. Brady, P. D. Brennan, and J. Kelly, "A robust method for microwave fet parameter extraction based on cold and hot s-parameters," in *2008 38th European Microwave Conference*. IEEE, 2008, pp. 380–383.